

The diagram illustrates the architecture of an ATM network. It consists of the following components and connections:

- FR Communication Module (PIM):** This module is connected to the network interface. It contains:
 - PHY (Physical Interface):** Receives multiple $E1/DS1$ signals.
 - FRCC (Frame Relay Communication Controller):** Manages the communication with the PIM.
- SAR/ALM Module:** This module is connected to the PIM via a **Utopia** interface. It contains:
 - SAR (Segmentation/Channeling Unit):** Processes data from the PIM.
 - ALM (ATM Adaptation Layer):** Manages the adaptation of data to the ATM network.
- Central Computer (FP):** The main processing unit, connected to the SAR/ALM module.
- Buffer Memory (PSSM):** Provides buffer memory for the network, connected to the Central Computer (FP).

FIG 2

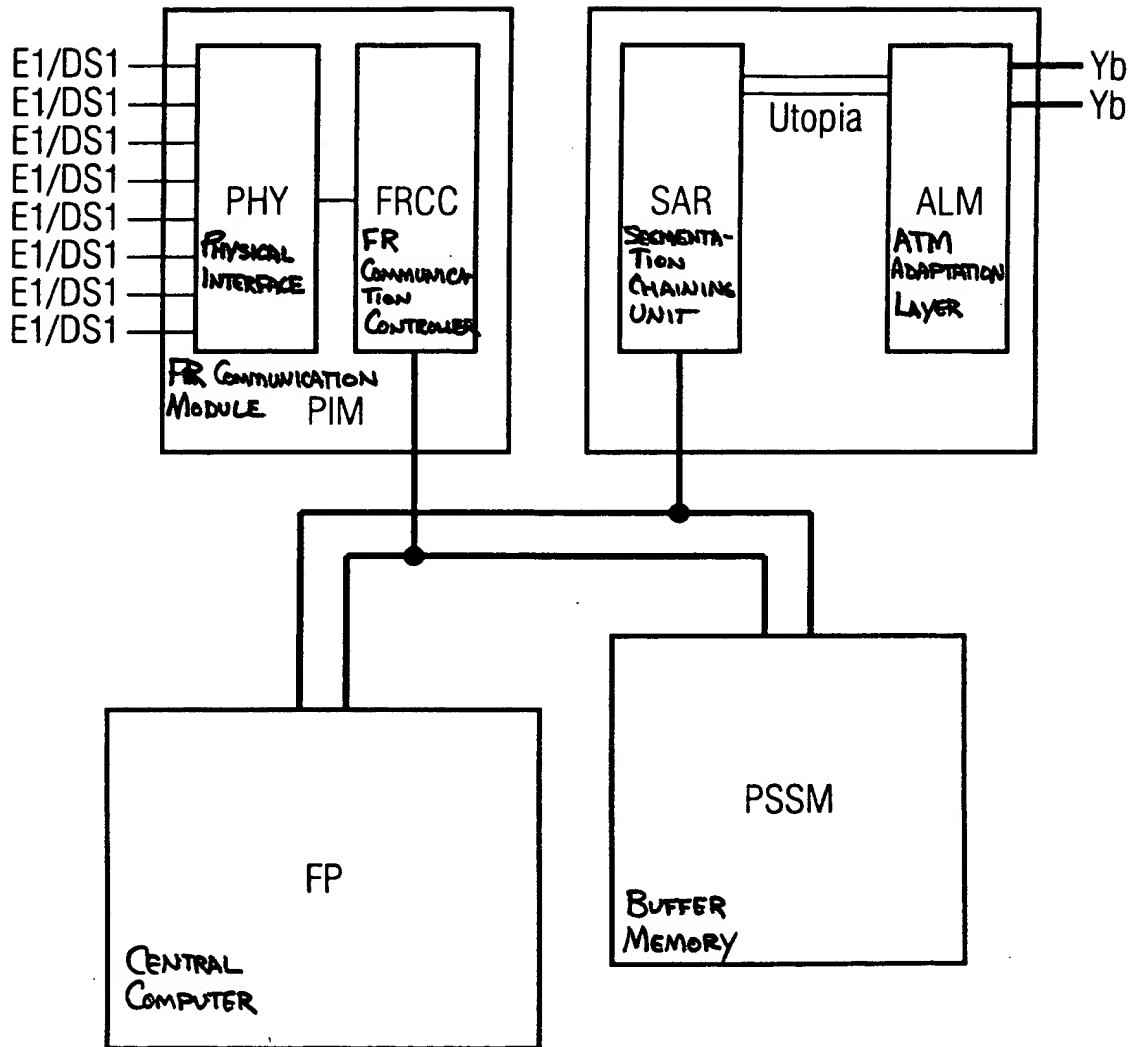
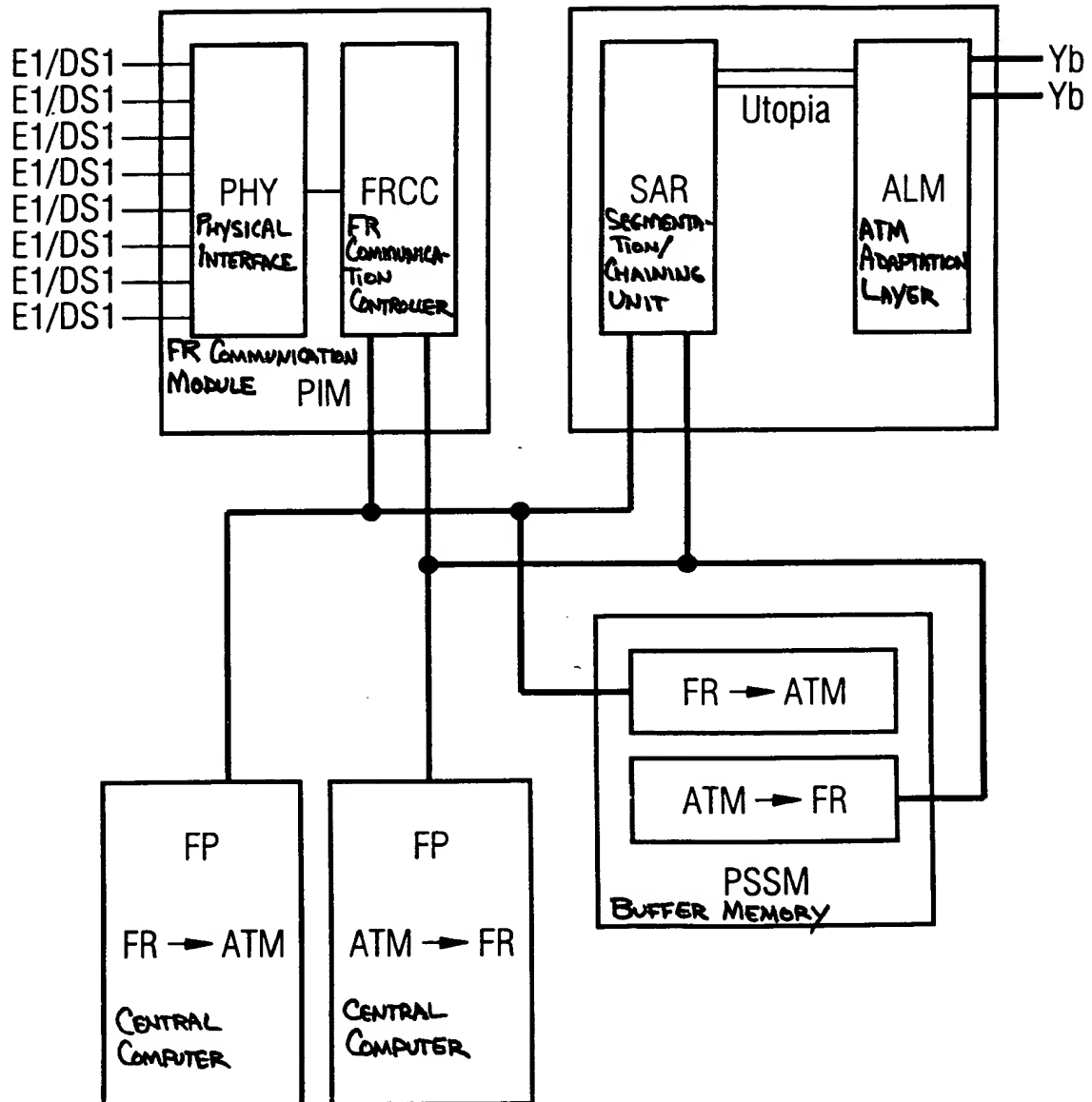
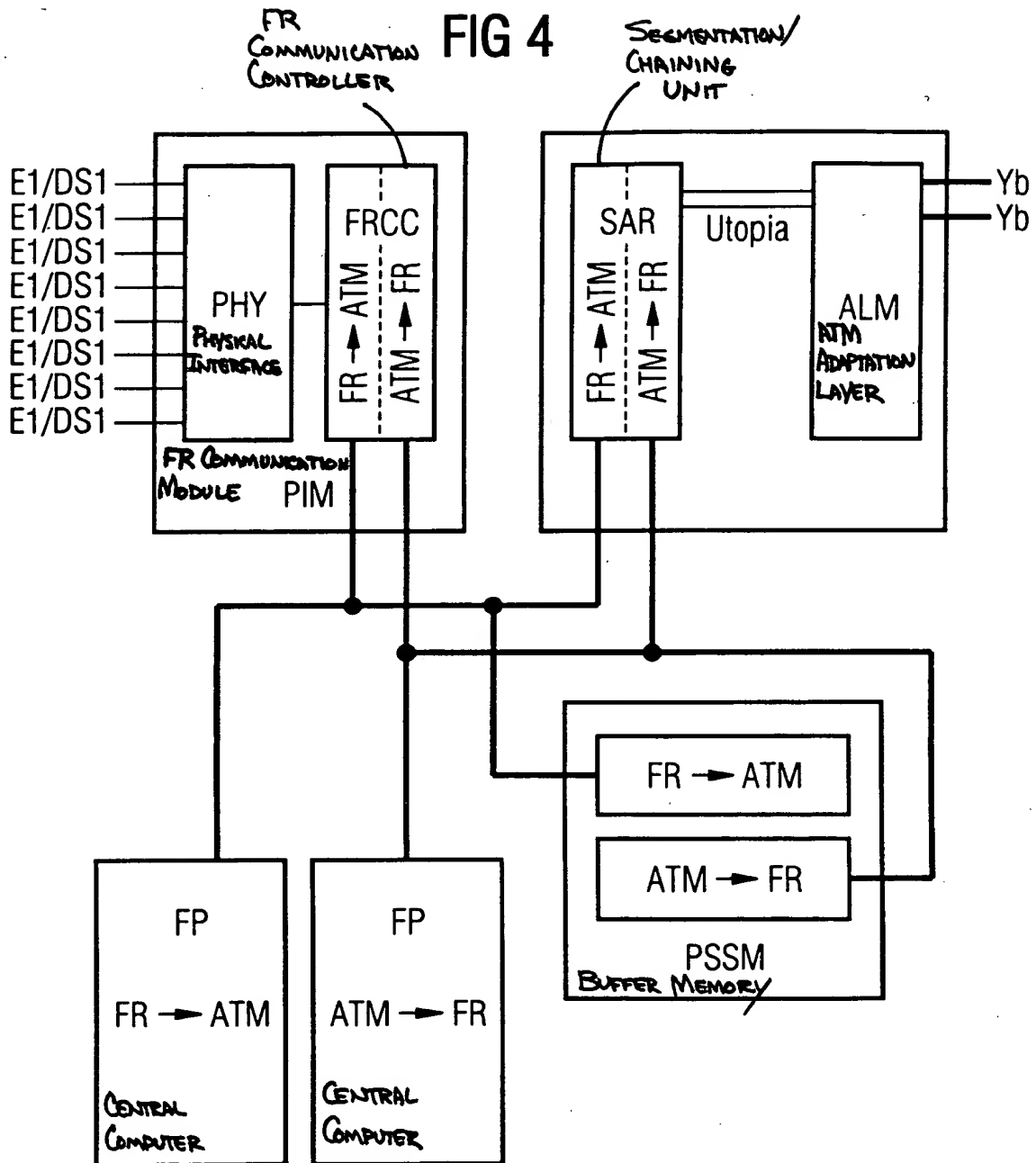


FIG 3





FR COMMUNICATION CONTROLLER

SEGMENTATION/ CHAINING - UNIT

